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Date: January 26, 2006

In re Application of: Benayoun, et al. ***Filed:*** 12/28/2001

For: Self-Route Expandable Multi-Memory Packet Switch with Distributed Scheduling Means

Serial Number: 09/683,429

Art Unit: 2662 ***Examiner:*** Dmitry Levitan

Response and Amendment Under 37 C.F.R. §1.111
And Petition for One Month Extension of Time Under 37 CFR 1.136(a)(1)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Office Action mailed on September 30, 2005, which was due for response by December 30, 2005. Applicants request a one month extension of time by virtue of the present response. Please charge Applicants' deposit account, 09-0456, a fee of $120 for a one month extension of time which is due by virtue of this response, and for any additional fee that the PTO determines is due.

It is respectfully requested that this Amendment be entered in the above referenced application and reconsideration of the application in view of the following remarks and amendments be made. No new matter has been included. The application should be amended as follows:

In the Drawings

The Office Action stated an objection to Figures 3-8 as failing to comply with 37 CFR 1.121(d) because descriptive labels necessary for understanding the drawings are missing. The Office Action also stated that the quality of the connections shown on Figure 8 is not acceptable. A proposed set of drawings to overcome the objections is attached to this amendment as Appendix A. Each sheet has been labeled "Replacement Sheet" to be in compliance with 37 CFR 1.121(d).

Therefore, Applicants respectfully submit that the objection to the drawings has been overcome.

In the Claims

Amend claim 1 as follows:

1. (Currently Amended) Data transmission system having a plurality of Local Area Networks (LANs) interconnected by a hub including a plurality of LAN adapters respectively connected to the plurality of LANs, the data transmission system comprising:

a packet switch interconnecting the plurality of LAN adapters wherein a packet transmitted by any one of the plurality of LAN adapters to the packet switch includes a header containing at least the address of the adapter to which the packet is forwarded, the packet switch includes a plurality of input ports and a corresponding plurality of output ports both being respectively connected to the plurality of LAN adapters, each pair of input port and output port defining a cross point;

the packet switch comprises:

a plurality of memory blocks, each memory block ~~located at each cross point~~ associated with one of said cross points for storing any data packet which is received from the input port corresponding to the cross point and which is to be forwarded to the output port corresponding to the cross point, and

a plurality of schedulers, each scheduler associated ~~with each output port~~ with one of said output ports for selecting at each ~~clock time~~ clock cycle a memory block among all memory blocks corresponding to the output port and causing the memory block to forward the stored data packet to the output port when predetermined criteria are met.

2. (Original) Data transmission system according to claim 1, wherein the memory block located at each cross point of the switch module includes a data memory unit for storing at least a data packet and a first memory controller which determines from the header of the received data packet whether the packet is to be forwarded to the output port associated

with the cross point and for storing the data packet into the data memory unit in such a case.

3. (Original) Data transmission system according to claim 2, wherein the memory block includes a header validation control block for determining whether the header of a data packet received from the input port contains the address of the output port associated with the cross point and the first memory controller which stores the data packet into the data memory unit if the header contains the address of the output port and for reading the data packet to forward it to the output port.

4. (Original) Data transmission system according to claim 3, wherein the scheduler sends a validation signal to the header validation control block to authorize the first memory controller to store the data packet into the data memory unit.

5. (Original) Data transmission system according to claim 4, further comprising an output data block connected to each output port which stores a data packet received from any memory block and transmits the data packet to the output port under the control of the scheduler.

6. (Original) Data transmission system according to claim 5, wherein the output data block includes a data selection block which validates the data packet after receiving a validating signal from the scheduler, an output memory unit which stores the data packet and a second memory controller which controlls the operation of storing the data packet into the output memory unit and the operation of reading the output memory unit for transmitting the data packet to the output port.

7. (Original) Data transmission system according to claim 6, wherein the packet switch includes a plurality of switch modules and wherein each down switch module includes for each output port an input expansion data block for buffering a data packet received from an expansion bus in connected to an up switch module and corresponding to the same output port as the output port of the down switch module.

8. (Original) Data transmission system according to claim 7, wherein the input expansion data block includes an expansion memory unit which buffers the data packet received from the expansion bus in, a header validation block which determines whether the header of the data packet contains the address of the output port associated with the cross point, and a third memory controller which stores the data packet into the expansion memory unit and reads the expansion memory unit to forward the data packet to the output port of the down switch module.

9. (Original) Data transmission system according to claim 8, wherein the scheduler sends a validation signal to the header validation block to authorize the third memory controller to store the data packet into the expansion memory unit.

10. (Original) Data transmission system according to claim 1, wherein an overflow signal is sent by the memory block to the scheduler when the memory block overflows.

11. (Original) Data transmission system according to claim 10, further comprising an overflow bus to transport the data packet to the memory block corresponding to the output port that after the scheduler has prevented the data packet from being stored into the memory block which overflows and has selected and validated another memory block which does not overflow.

12. (Original) Data transmission system according to claim 10, further comprising a back-pressure mechanism which sends back-pressure signals to input adapters to request the input adapters to reduce the flow of the data packets transmitted to the packet switch when there is too much overflow detected by each scheduler of the packet switch.

13. (Original) Data transmission system according to claim 12, further comprising an overflow mechanism adapted to receive overflow control signals from the schedulers of the packet switch when there is too much overflow and to transmit an overflow signal to the back-pressure mechanism.

14. (Original) Data transmission system according to claim 1, wherein the header of the data packet includes two bytes in which the first byte contains an identification field (unicast, multicast) and the second byte contains a module address field when the packet switch comprises several packet switch modules.

Remarks

Claims 1-14 are pending in this action. Claims 1-14 stand rejected. By this amendment claim1 has been amended. Applicants respectfully request reconsideration of all pending claims herein.

Claim Objections

The Office Action stated that Claims 1 – 14 are objected to because "a memory block located at each of the cross points" is unclear because memory location seems to be irrelevant in the claim, contrary to the memory connection/association to the ports as claimed. Applicants have amended Claim 1 to clarify that a memory block is associated with an input port and an output port and is not dependent on physical location. Claim 1 now reads, "…wherein the packet switch comprises a plurality of memory blocks, each memory block associated with one of said cross points …".

Therefore, Applicants believe that the objection to claims 1-14 has been overcome.

Claim Rejections - 35 U.S.C. § 112, second paragraph

The Office Action stated that claims 1-14 are rejected under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as his invention. Specifically, for Claim 1, the Office Action stated that it was unclear as to what output and input ports are considered a pair and what is the definition of a cross point. Applicants submit that the definition of "cross point" is defined in paragraph 10 of the specification as "each couple of an input port and an output port defining a cross point within the switch module" and is shown in Figures 1, 3, 5, and 8. In Figure 1, the input and output ports are shown as the input buses 13_1 – 13_4 and corresponding output busses 15_1 – 15_4 coupled

to the packet switch module 14. A pair is therefore any one of the input ports (i.e. input bus 13) coupled to any one of the output ports (i.e. output bus 15). For example, one cross point is input bus 13_1 coupled to output bus 15_4, or input bus 13_2 coupled to output bus 15_3, etc. Thus, for 4 input ports and 4 output ports there is a total of 16 cross points. In Figure 3 the cross point is shown as the intersection of elements 50 and 60, which are coupled to data bus in 13 and data bus out 15 respectively (see paragraph 27). Memory Block 200 is associated with the cross point shown in Figure 3. Figure 5 shows a block diagram of Memory Block 200 with the intersection of elements 50 and 60 showing the cross point. Figure 8 shows multiple cross points for input ports 13_1 – 13_m and output ports 15_1 – 15_m and represents an mxm number of cross points with associated memory blocks 200 for each cross point.

The Office Action stated that the limitation in claim 1 of "… selecting at each clock time …" is unclear because it is not understood when the selection should occur, as there are no time units associated with "each clock time". Applicants have amended Claim 1 to replace "each clock time" with "each clock cycle", which is a well-known term in the networking and computer industries.

Based on the foregoing arguments and amendments, Applicants believe that the rejection to Claims 1 – 14 under 35 U.S.C. §112, second paragraph, has been overcome.

Claim Rejections - 35 U.S.C. § 103(a)

The Office Action stated that claims 1, 2 and 10 are rejected under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent No. 6,205,145 issued to Yamazaki.

Applicants respectfully submit that the present invention is patentable over U.S. Patent No. 6,205,145 issued to Yamazaki because Yamazaki does not teach or suggest the limitation of Applicants' claim 1, as amended, of " … the packet switch comprises a plurality of memory blocks,

each memory block associated with one of said cross points … ". Support for Applicants' claim 1, as amended, can be found, for example, in paragraph 0025 and Figure 3.

The combination of input and output buffer means shown as 20-23 and 30-33 respectively on Fig. 5 of the Yamazaki reference are not cross points because there is no provision for each input/output buffer combinations to coordinate one-to-one with every termination node input/output node combination. Yamazaki does not teach a memory block for each of the cross points because cell producing means 40-43 does not include a first memory controller which determines from the packet header whether the packet is to be forwarded to the output port associated with the cross point. Rather, the frame division control section 143 of Figure 8 (referred to in the Office Action) serves to divide an incoming packet into fixed length cells, interchange the cells and, reconstruct the original frame from the interchanged cells (See Yamazaki Abstract, Summary, Claims 1, 6, 10, 16, 26, and 29, Figure 8, and 10:57-11:4). The output buffer requirement control section 144 of Figure 8 sends command signals the frame division control 143 according to inputs from the congestion control bus 180 (See Yamazaki 10:14-26, and Figures 6 and 8). Neither the output buffer requirement control section 144 nor the frame division control section 143 determine from the packet header whether the packet is to be forwarded to the output port associated with the cross point as taught by the Applicants' instant invention.

Applicants respectfully submit that Yamazaki does not teach or suggest the limitation of Applicants' claim 1, as amended, of "…a plurality of schedulers, each scheduler associated with one of said output ports …". Support for Applicants' claim 1, as amended, can be found, for example, in paragraphs 0008, 0026, 0051, 0052 and Figures 3 and 8.

Referring to Figure 5 of Yamazaki, Yamazaki teaches a <u>single</u> congestion control means 70 associated with a plurality of frame construction means 50-53 and, indirectly, a plurality of output data buffer means 30-33. Yamazaki's congestion control means 70 is unique and centralized in the fibre channel fabric so the congestion control means 70 must know the complete switching topology of the system in order to control packet flow. Yamazaki is silent on teaching or suggesting a plurality of congestion control means, each congestion control means associated with one of the output data buffer means.

Therefore, Applicants believe that the rejection of Claims 1, 2 and 10 under 35 U.S.C. §103(a) has been overcome.

Conclusion

Based on the foregoing, it is respectfully submitted that the pending claims in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
For: Alain Benayoun, et al.

By: _____

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Appendix A

Proposed Drawings 1 - 9 (9 sheets)

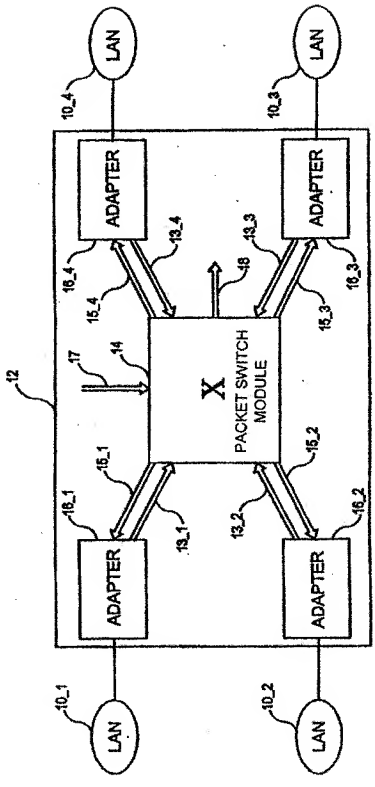
LAN
LAN
10_4
10_3
ADAPTER
ADAPTER
13_4
13_3
16_4
15_4
18
15_3
16_3
17
14
12
X
PACKET SWITCH
MODULE
15_1
15_2
18_1
16_2
13_1
13_2
ADAPTER
ADAPTER
10_1
10_2
LAN
LAN

FIG. 1

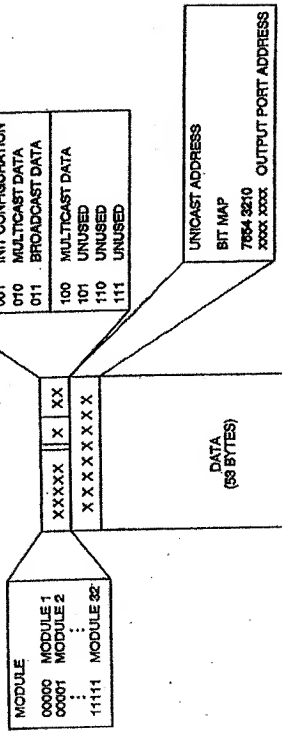
MODULE
00000 MODULE 1
00001 MODULE 2
11111 MODULE 32
XXXXX
X
XX
XXXXXXXX
DATA
(33 BYTES)
000 IDENTIFICATION
001 UNICAST DATA
010 INIT CONFIGURATION
011 MULTICAST DATA
100 BROADCAST DATA
101 MULTICAST DATA
110 UNUSED
111 UNUSED
UNUSED
UNUSED
UNICAST ADDRESS
BIT MAP
7654 3210
XXXX XXXX OUTPUT PORT ADDRESS

FIG. 2

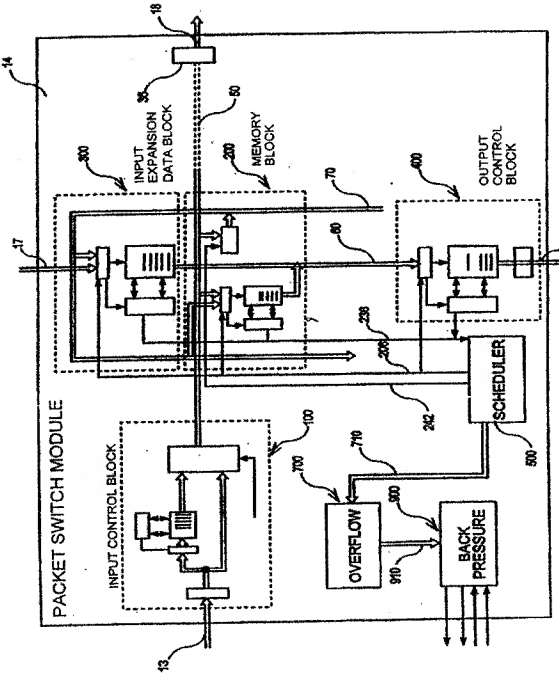
PACKET SWITCH MODULE
INPUT CONTROL BLOCK
INPUT EXPANSION DATA BLOCK
MEMORY BLOCK
OUTPUT CONTROL BLOCK
SCHEDULER
OVERFLOW
BACK PRESSURE
14
18
35
50
300
200
70
400
17
60
15
230
240
242
100
710
700
500
600
910
13

FIG. 3

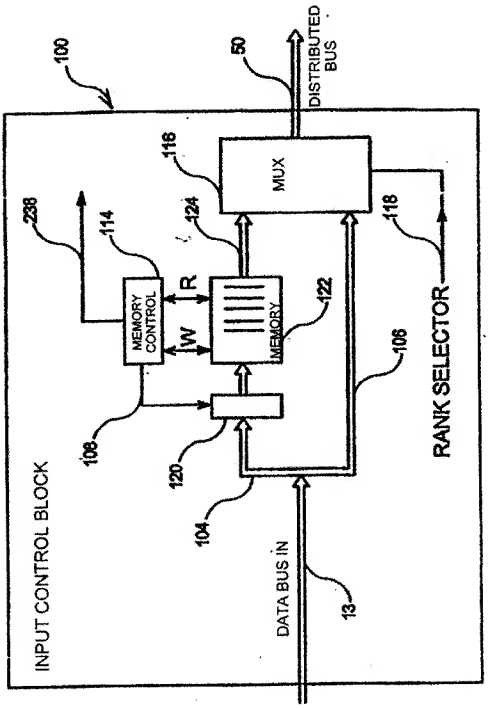
100
50
DISTRIBUTED BUS
116
MUX
238
114
124
118
R
W
MEMORY CONTROL
122
MEMORY
106
RANK SELECTOR
108
120
104
INPUT CONTROL BLOCK
DATA BUS IN
13

FIG. 4

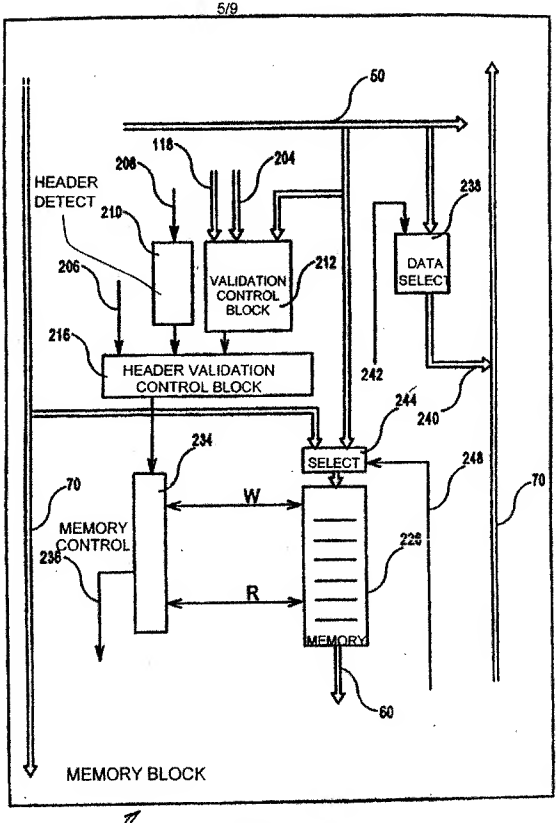
50
118
208
204
HEADER
DETECT
210
238
206
VALIDATION
CONTROL
BLOCK
212
DATA
SELECT
216
HEADER VALIDATION
CONTROL BLOCK
242
244
240
234
SELECT
248
70
70
W
MEMORY
CONTROL
226
236
R
MEMORY
60
MEMORY BLOCK
200

FIG. 5

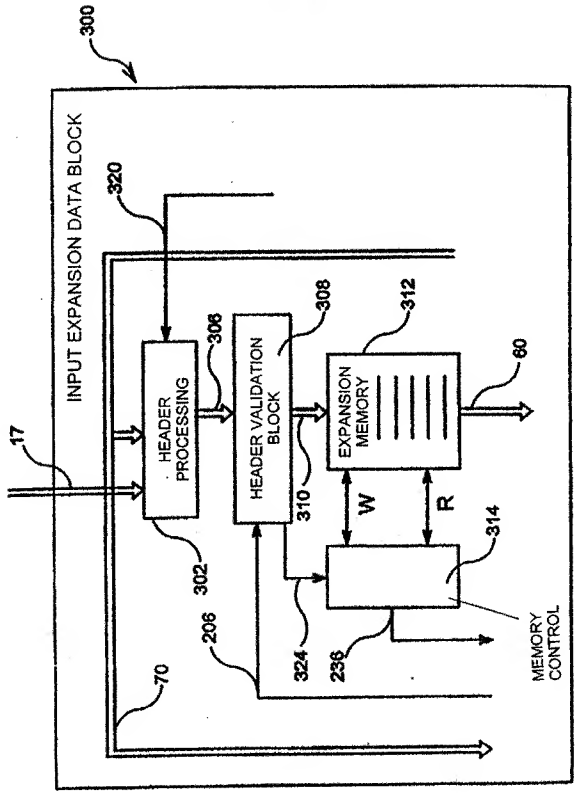
300
INPUT EXPANSION DATA BLOCK
320
17
HEADER PROCESSING
306
HEADER VALIDATION BLOCK
308
310
EXPANSION MEMORY
312
60
W
R
314
MEMORY CONTROL
302
206
324
236
70

FIG. 6

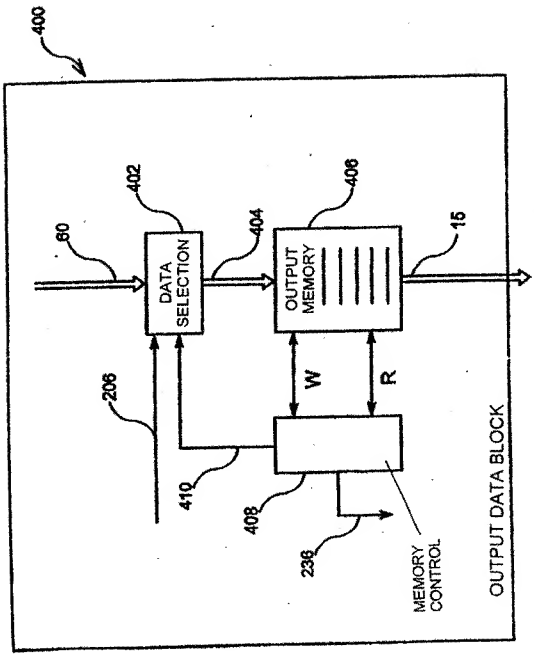
400
402
60
DATA SELECTION
404
406
OUTPUT MEMORY
15
206
W
R
410
408
236
MEMORY CONTROL
OUTPUT DATA BLOCK

FIG. 7

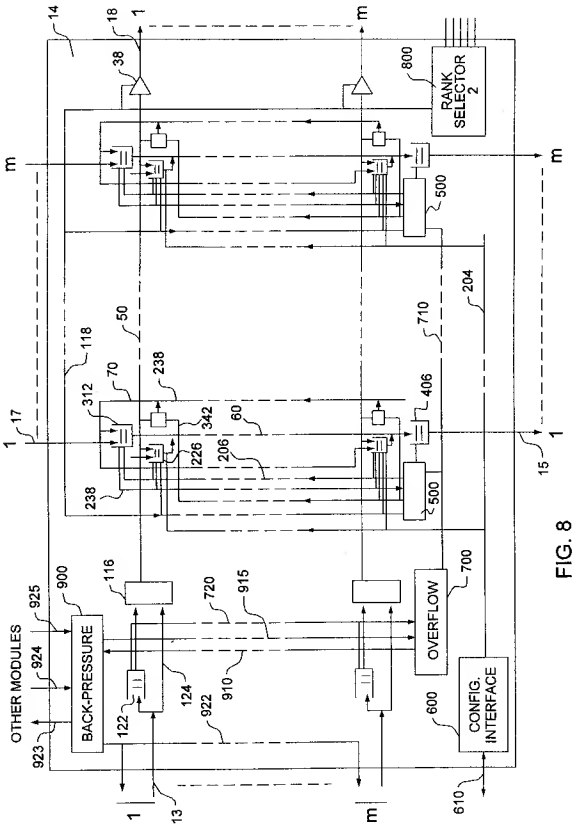
14
18
1
m
38
800
RANK SELECTOR 2
500
204
710
406
50
118
70
238
312
342
60
226
206
17
15
OTHER MODULES
925
924
923
900
BACK-PRESSURE
116
122
124
720
915
910
922
OVERFLOW
700
600
CONFIG. INTERFACE
610
13

FIG. 8

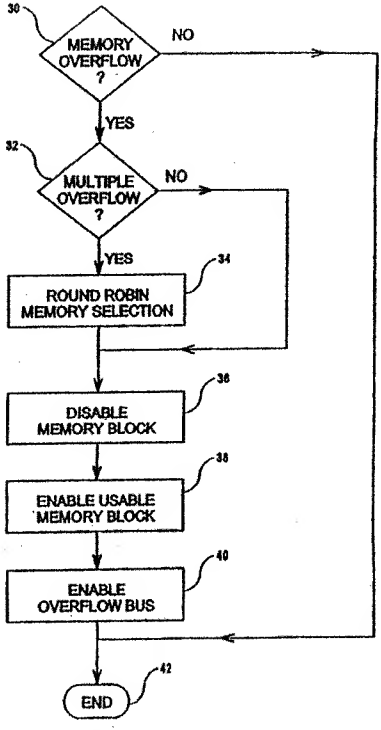
30
MEMORY OVERFLOW ?
NO
YES
32
MULTIPLE OVERFLOW ?
NO
YES
34
ROUND ROBIN MEMORY SELECTION
36
DISABLE MEMORY BLOCK
38
ENABLE USABLE MEMORY BLOCK
40
ENABLE OVERFLOW BUS
42
END

FIG. 9